THE INVENTION CLAIMED IS:

1. A method of assembling a semiconductor package for a large die comprising:

providing a die pad and a plurality of bonding fingers;

attaching a spacer to the die pad;

attaching the large die to the spacer;

wire bonding a plurality of wires between the large die and the plurality of bonding fingers; and

encapsulating the die pad, the plurality of bonding fingers, the spacer, the large die and the plurality of wires.

2. The method as claimed in claim 1 wherein attaching the spacer attaches a conductive material having a thickness in the range of about 100 microns to about 300 microns.

3. The method as claimed in claim 1 wherein attaching the large die attaches the large die overlapping the inner edge of the plurality of bonding fingers.

4. The method as claimed in claim 1 wherein:

providing the plurality of bonding fingers includes providing a plurality of contacts pads thereon; and

attaching the large die attaches the large die at least partially overlapping the plurality of contact pads.

5. The method as claimed in claim 1 wherein wire bonding the large die attaches a wire having a substantially 90° angle bend between the die and the plurality of bonding fingers.

6. A method of assembling a semiconductor package for a large die comprising:

providing a die pad, a plurality of inner bonding fingers and a plurality of outer bonding fingers;

attaching a spacer to the die pad;

attaching the large die to the spacer;

wire bonding a plurality of wires between the large die and the plurality of inner bonding fingers and the plurality of outer bonding fingers; and

encapsulating the die pad, the plurality of outer bonding fingers, the plurality of inner bonding fingers, the spacer, the large die, and the plurality of wires.

7. The method as claimed in claim 6 wherein attaching the spacer attaches a conductive material having a thickness in the range of about 100 microns to about 300 microns.

8. The method as claimed in claim 6 wherein attaching the large die attaches the large die overlapping the inner edge of the plurality of inner bonding fingers.

9. The method as claimed in claim 6 wherein:

providing the plurality of inner bonding fingers includes providing a plurality of contacts pads thereon; and

attaching the large die attaches the large die at least partially overlapping the plurality of contact pads.

10. The method as claimed in claim 6 wherein assembling the semiconductor package comprises assembling a quad flat-packed non-leaded package, a leadframe ball grid array package, or a combination thereof.

11. A semiconductor package for a large die comprising:

a die pad;

a plurality of outer bonding fingers;

a spacer attached to the die pad;

a large die attached to the spacer;

bonding wires bonded between the large die and the plurality of bonding fingers; and

an encapsulant to encapsulate the die pad, the plurality of bonding fingers, the spacer, the large die, and the bonding wires.

12. The semiconductor package as claimed in claim 11 wherein the spacer is a conductive material having a thickness in the range of about 100 microns to about 300 microns.

13. The semiconductor package as claimed in claim 11 wherein the large die overlaps the inner edges of the bonding fingers.

14. The semiconductor package as claimed in claim 11 wherein:

the plurality of bonding fingers have a plurality of contact pads thereon; and

the large die at least partially overlaps the plurality of contact pads.

15. The semiconductor package as claimed in claim 11 wherein the bonding wires have a substantially 90° angle bend.

16. A semiconductor package for a large die comprising:

a die pad;

a plurality of inner bonding fingers;

a plurality of outer bonding fingers;

a spacer attached to the die pad;

a large die attached to the spacer;

a plurality of bonding wires connected between the large die and the plurality of inner bonding fingers and the plurality of outer bonding fingers; and

an encapsulant to encapsulate the die pad, the plurality of inner bonding fingers, the plurality of outer bonding fingers, the spacer, the large die, and the plurality of bonding wires.

17. The semiconductor package as claimed in claim 16 wherein the spacer a conductive material having a thickness in the range of about 100 microns to about 300 microns.

18. The semiconductor package as claimed in claim 16 wherein the large die overlaps the inner edge of the plurality of inner bonding fingers.

19. The semiconductor package as claimed in claim 16 wherein:

the plurality of inner bonding fingers have a plurality of contact pads thereon; and

the large die at least partially overlaps the plurality of contact pads.

20. The semiconductor package as claimed in claim 16 wherein the semiconductor package is a quad flat-packed non-leaded package, a leadframe ball grid array package, or a combination thereof.